REMARKS

Applicant thanks the Office for its indication that claims 4-6, 10-12 and 16-18 contain allowable subject matter. In response to the above-identified Office Action, Applicants have amended claims 1, 7 and 13 and added claims 19-21. Support for the amendments to the claims and the added claims can be found in the specification for the above-identified application at page 9, lines 12-20. Accordingly, no new matter has been entered by way of these amendments. In view of these above amendments and the following remarks, Applicants hereby request further examination and reconsideration of the application, and allowance of claims 1-21.

The Office has rejected claims 1-3, 7-9 and 13-15 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,441,184 to Sonoda et al. ("Sonoda"). The Office asserts that Sonoda discloses a system and method of interleaving data comprising determining a first position of elements of data in an interleaved sequence using a second position of the elements in a source sequence and a number of elements to be skipped (col. 5, lines 47-53; FIGS. 3 and 5; one element is skipped to allow the odd and even numbered data words to be adjacent); interleaving the elements of data in the source sequence according to the determined first position of the elements to form the interleaved sequence, wherein adjacent elements in the interleaved sequence originally were separated by a first number of elements in the source sequence and originally adjacent elements in the source sequence are separated by at least a second number of elements in the interleaved sequence (col. 1, lines 37-55); and transmitting the interleaved sequence of the elements of the data (col. 3, lines 1-25). In response, Applicants have amended claims 1, 7 and 13 as shown herein and submit the following remarks.

Sonoda does not suggest or disclose, "wherein adjacent elements in the interleaved sequence originally were separated by a first number of elements in the source sequence ... wherein the first number is adjustable," as recited in claims 1, 7 and 13. Applicants respectfully direct the Office's attention to Sonoda at FIGS. 3 and 5; and col. 5, lines 47-51, which disclose a signal being supplied into an odd-even separating circuit 2 that separates the signal into odd data sequences W(1), W(3) and W(5) and even data sequences W(2), W(4) and W(6). The odd and even data sequences together with a first parity data sequence P(1) are sent to a first interleaving stage 4 that imparts a set of delay times into the entire sequence, as disclosed at col. 5, line 64 through col. 6, line 6. Thereafter, the entire

sequence together with a second parity data sequence Q(1) is sent to a second interleaving stage 6 that imparts another set of delay times into the entire sequence, as disclosed at col. 6, lines 12-25. The resulting interleaved and data and parity word sequences are applied to an assembling circuit 7 which provides at an output 8 a stream of transmission blocks, as illustrated in FIG. 5 and described col. 6, lines 25-32. However, Sonoda does not disclose or suggest that the number of data sequences the odd-even separating circuit 2 skips in the original signal before adding a data sequence from the original signal into the interleaved sequence is adjustable, as claimed. As acknowledged by the Office, the number of sequences in the original signal that are skipped never changes, since one data sequence in the original signal is skipped for the odd interleaved data sequence and one data sequence is skipped for the even interleaved data sequence.

As discussed at page 6, lines 24-26, in the above-identified application, if data packets are not interleaved before transmission, the loss of sequential data packets results in the loss of a large amount of contiguous data. However, interleaving data must not introduce more latency than is tolerable by end users and must separate contiguous data sufficiently far apart to make the interleaving scheme effective, as disclosed at page 7, lines 17-19 in the above-identified application. Prior interleaving methods, such as the method disclosed in Sonoda, introduce delays into interleaved data to sufficiently separate the data sequences which were contiguous in the original signal. In contrast, the present invention ensures the data sequences in an interleaved sequence (which were contiguous in the original source sequence) are sufficiently separated by controlling the order of the data sequences in the interleaved sequence using an adjustable skip value, rather than relaying on introducing delays in the interleaved sequence, as disclosed at page 8, lines 20-25 in the above-identified application. Further, the adjustable skip value enables the present invention to adapt to changing data transmission environments and/or to be applied to a variety of data transmission environments with differing needs with respect to the amount of separation needed for data sequences in an interleaved sequence that were contiguous in the original source sequence.

As discussed at page 3, lines 14-18 in the above-identified application, the value representing the number of data packets to be skipped (e.g., K) can be changed "on the fly" in real-time applications to adapt to changing environments, whereas other systems (e.g.,

Sonoda) always arrange the interleaved data in a particular manner resulting in an inflexible system. This enables the present invention to effectively interleave data to be transmitted without introducing additional delays. Thus, the present invention provides a faster and more flexible and efficient alternative to prior error correction schemes as disclosed at page 3, lines 9-18. In view of the foregoing amendments and remarks, the Office is respectfully requested to reconsider and withdraw the rejections of claims 1, 7 and 13. Since claims 2-6 and 19 depend from and contain the limitations of claim 1, claims 8-12 and 20 depend from and contain the limitations of claim 7, and claims 14-18 and 21 depend from and contain the limitations of claim 13, they are patentable in the same manner as claims 1, 7 and 13.

Additionally, Sonoda does not suggest or disclose, "wherein the adjustable first number is changed to avoid interleaving one of the elements of data from the source sequence into the interleaved sequence that has already been interleaved into the interleaved sequence," as recited in claims 43-45. As described above in connection with Sonoda at FIGS. 3 and 5; and col. 5, lines 47-51, a signal is sent into an odd-even separating circuit 2 to form odd data sequences W(1), W(3) and W(5) and even data sequences W(2), W(4) and W(6), the sequences and a first parity data sequence P(1) are sent to a first interleaving stage 4 that imparts a set of delay times into the entire sequence, the entire sequence together with a second parity data sequence Q(1) are sent to a second interleaving stage 6 that imparts another set of delay times into the entire sequence, and the resulting interleaved data and parity word sequences are applied to an assembling circuit 7 which provides at an output 8 a stream of transmission blocks shown in FIG. 5, as disclosed at col. 5, line 64 through col. 6, line 6; col. 6, lines 12-25; and col. 6, lines 25-32.

However, the odd-even separating circuit 2 in Sonoda will never need to deal with the situation where the number of elements to be skipped must be changed to avoid interleaving one of the data sequences from the original signal into the interleaved sequence that has already been interleaved into the interleaved sequence since the circuit 2 only separates the signal into an odd data sequence W(1), W(3) and W(5) and an even data sequences W(2), W(4) and W(6). Furthermore, the Office has acknowledged that the value representing the number of elements to be skipped in Sonoda never changes since one data sequence in the signal supplied to the circuit 2 is skipped for the odd interleaved data sequence and one data sequence is skipped for the even interleaved data sequence.

As discussed at page 9, lines 12-20 in the above-identified application, some elements may be selected from the input sequence more than once and some elements may be missed. Thus, the present invention changes the skip value ("K") when an element from the input sequence has already been selected, as in the case where the K value is not relatively prime with respect to the number of elements being interleaved (e.g., N), as discussed at page 9, lines 12-20 in the above-identified application. Thus, the present invention adjusts the number of elements to be skipped (e.g., K), such as by incrementing the K value by one when an element is about to be selected a second time. As discussed at page 3, lines 14-18 in the above-identified application, the number of data packets to be skipped (e.g., K) can be also changed "on the fly" in real-time applications to adapt to changing environments, whereas other systems (e.g., Sonoda) always arrange the interleaved data in a particular manner resulting in an inflexible system.

This enables the present invention to effectively interleave data to be transmitted. As discussed at page 6, lines 24-26, in the above-identified application, if data packets are not interleaved before transmission the loss of sequential data packets results in the loss of a large amount of contiguous data. Thus, the present invention provides a faster and more flexible and efficient alternative to prior error correction schemes as disclosed at page 3, lines 9-18. In view of the foregoing amendments and remarks, the Office is respectfully requested to reconsider and withdraw the rejections of claims 1, 7 and 13. In view of the foregoing remarks, Applicant respectfully submits that claims 43-45 are distinguishable over the cited references and are patentable for these additional reasons.

In view of all of the foregoing, it is submitted that this case is in condition for allowance and such allowance is earnestly solicited. In the event that there are any outstanding matters remaining in the above-identified application, the Office is invited to contact the undersigned to discuss this application.

Respectfully submitted,

Certificate of Mailing - 37 CFR 1.8(a)
Date: February 28, 2004
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: MailStop RCE Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450, on the date below.
Date 2-28 John Campa

John Campa
Registration No. 49,041

NIXON PEABODY LLP
Clinton Square, P.O. Box 31051
Rochester, New York 14603-1051
Telephone: (585) 263-1519
Facsimile: (585) 263-1600